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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3 :
H03K 6/04, G01R 19/165
H03L 7/00

A1

(11) International Publication Number: WO 85/ 0523

(43) International Publication Date:
21 November 1985 (21.11.85

(21) International Application Number: PCT/US85/00524

(22) International Filing Date: 28 March 1985 (28.03.85)

(31) Priority Application Number: 607,998

(32) Priority Date: 7 May 1984 (07.05.84)

(33) Priority Country: US

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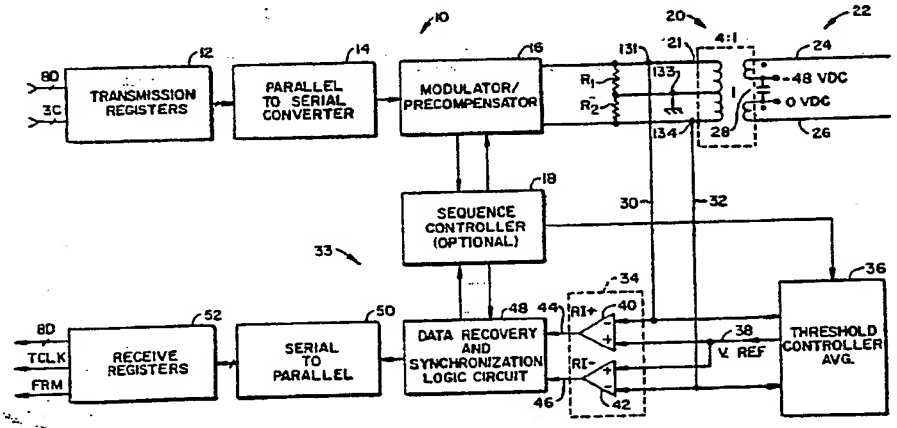
(81) Designated States: AT (European patent), AU, BE (European patent), BR, CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: HIGH-SPEED DIGITAL LOOP TRANSCEIVER



(57) Abstract

A high-speed digital transceiver (10, 33) for use in a PBX environment comprising twisted-pair wire cables (22) interconnecting like transceivers, each transceiver being operative to exchange voice, data and control information in a packetized format over a common twisted-pair cable (22). Specifically, each transceiver communicates packetized pulse code modulated information in pure Alternate Mark Inverted (AMI) coding (200), that is, without the introduction of bipolar violation pulses to provide timing. Frame synchronization is acquired on the first pulse by the use of a digital circuit (48) deriving synchronization from a local high-speed clock (54). The use of a high-speed clock-driven digital circuit for synchronization acquisition eliminates the need for a phase-locked loop synchronization scheme and its concomitant finite acquisition delay. In addition, a receiving section (33) employs a threshold selecting circuit (62) which switches or makes thresholds in response to an expectation of the absence any bipolar violation in the transmitted signal. The effect of inter-symbol interference are further minimized by provision of digital precompensation (16) in the transmitted signal to maximize the slew rate between consecutive pulses. The precompensation scheme is based on a knowledge of the bit pattern and the amount of energy contained in a sequence of bits.

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HIGH-SPEED DIGITAL LOOP TRANSCEIVER

BACKGROUND OF THE INVENTION

This invention relates to digital telecommunications and more particularly to digital telecommunications in the megabit/second data rate range using a standard telephone twisted-pair cable a few thousand feet in length. The invention is primarily for use in local loop digital subscriber telephone systems capable of supporting voice, data and image transmission. However, apparatus according to the invention may also be used in connection with data acquisition and digital control tasks.

The transmission of information in digital form at frequencies exceeding one megabit/second has in the past generally been accomplished by means of expensive cabling systems, such as coaxial cable, shielded twisted-pair cable, for fiberoptic cable. In the past, such systems have generally required sophisticated data recovery techniques including analog equalization and phase synchronization.

While the use of such known techniques can be justified for communication between computer equipment where expense is not a primary factor, there is nevertheless a need to provide a relatively inexpensive and yet reliable system optimized for use with inexpensive, often previously installed, standard twisted-pair wiring. A transceiver for this purpose must not only meet economic criteria but also satisfy stringent bit error rate standards, radiation standards, and cross-talk standards.

There is a growing need to provide for the interface of telephones with various types of digital communication equipment, including personal computers and the like, to previously installed twisted-pair wiring. One possible technique for implementing shared voice and data communication is through the use of packet switching wherein

packets contain voice, data or control and signaling information. To be effective, packet switched communications must be at a rate high enough to allow transmission of voice signals with minimal delays in order to permit conversational communication. In a PBX environment where it is desired to minimize the number of wires, it is preferable to provide power over the same physical wires which carry data. This imposes the requirement that digital data be in an ac form free of dc offsets. The transmitters and receivers can thus be coupled to the transmission medium by means of pulse transformers, and data and coding schemes such as alternate mark inversion (AMI) must be employed. While AMI encoding schemes are appropriate for transformer coupled lines, AMI schemes are not self-clocking so synchronization is easily lost. The conventional solution is to provide modified AMI schemes are known to take into account arbitrarily long sequences of zeros which result in arbitrarily long periods between pulses. The modified schemes involve insertion of intentional bipolar violations in the data stream. Detection schemes for such systems are generally complex and expensive.

High frequency transmission system operating over distances exceeding a few hundred feet generally adopt a self-encoding scheme and employ phase locked loop synchronization techniques with continuous frequency and/or phase tracking. Phase locked loop synchronization techniques require a finite acquisition time at the beginning of each frame, so bandwidth constraints and delays seriously hinder use in a high-speed environment with frequent synchronization. Moreover, four wire systems are frequently required to achieve full duplex capability, since in prior art schemes, line turnaround is slowed by synchronization delays.

Another problem noted, particularly with the standard twisted-pair cabling over a length of several hundred feet, is the low pass filter effect caused by the

lines themselves. The medium dependent low pass filter characteristic causes distortion which increases the problem of intersymbol interference when data rates approach the bandwidth of the medium. In the past, the low pass filter characteristics have been compensated for at the receiving end of a channel by means of analog equalization to achieve acceptable bit error rates. Analog equalization does not lend itself to digital integration, thus reducing any advantages gained by large scale integration of other circuits. Still further, intersymbol interference imposes conflicting requirements on the level detection threshold used to distinguish between logic values ONE and ZERO. For example, the voltage threshold used to separate pulses from the absence of pulses is preferably as low as possible in order to compensate for effect of intersymbol interference. Transmission of a pulse followed by the absence of pulses may be detected incorrectly at the receiving end as consecutive pulses if the threshold voltage used to separate the pulses from the absence of pulses is set at a low value. This false reading is due to the relatively long discharge time of a transmission medium acting as a low pass filter. Straightforward detection schemes are further complicated because a DC free coding scheme such as AMI is non-self clocking. A clock signal is frequently embedded in an AMI code for synchronization purposes. Unfortunately a clock signal may create a DC artifact.

These and other problems have been addressed and overcome in the development of a high-speed digital transceiver suitable for voice and data interchange in a PBX environment.

SUMMARY OF THE INVENTION

A digital transceiver is provided to exchange voice and data via a packet protocol in a PBX environment. The environment comprises twisted wire cables interconnecting like transceivers communicating in the M bit/sec. range. Specifically, each transceiver

communicates packetized pulse code modulated information in pure Alternate Mark Inverted (AMI) coding. Frame synchronization is achieved by the use of a variable length, frequently synchronized window deriving synchronization from a high-speed counter driven by a high-speed clock. The use of a high-speed counter for synchronization eliminates the need for a phase-locked loop synchronization scheme and its concomitant finite phase acquisition delay. In addition, the receiving section of the transceiver employs means for selecting between threshold levels. Switching is effected in response to an expectation of the absence any bipolar violation in the transmitted signal. The effects of intersymbol interference are further minimized by provision of digital precompensation in the transmitted signal to maximize the slew rate between consecutive bits. The precompensation scheme is based on a knowledge of the bit pattern and the amount of energy contained in a sequence of bits.

The invention is implemented in a packetized full duplex two-wire voice and data communication system employing ping-pong protocol having a packet size compatible with the DS1 (T1) pulse code modulated data communication frame. Up to 16 bytes per 125 microsecond frame may be transmitted, the frame corresponding to maximum data rate of 1.024 M bit/sec. The actual transmission rate over a twisted-pair cable is on the order of 2 M bit/sec. so as to permit full duplex two-wire communication over a single twisted-pair cable. Full duplex capability is obtained by transmitting a burst of information in one direction at one frame and thereafter a burst of information in the opposite direction at the next frame. Synchronization must be renewed with each frame, and in the particular embodiment herein disclosed, every 125 microseconds. The use of a frame-synchronized clock based on a high-speed counter makes possible rapid synchronization on a frequent basis.

The invention will be better understood by reference to the following detailed description taken in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a transceiver in accordance with the invention.

Figure 2 is a schematic diagram of a portion of a receiver circuit according to the invention.

Figure 3 is a schematic diagram of a portion of a transmitter circuit having precompensation according to the invention.

Figure 4A is a waveform diagram of a transmitted waveform in accordance with the invention.

Figure 4B is a waveform diagram showing a received waveform with a variable threshold according to the invention.

Figure 4C is a waveform diagram which shows the data window signal during which data signals are considered valid.

Figure 5A is a waveform diagram showing the output waveform of the data or sync bit signal.

Figure 5B is a waveform diagram showing one portion of the frame or FRM signal.

Figure 5C is an exemplary clock signal.

Figure 5D is a waveform diagram of an exemplary data window signal equivalent to the waveform of Figure 4C.

Figure 5E is a waveform diagram representing an exemplary data output signal.

DESCRIPTION OF SPECIFIC EMBODIMENTS

Figure 1 shows a block diagram of a digital transceiver 10 according to the present invention. Input comprises eight data lines and three control lines coupled to a comensurate number of transmission registers 12; these transmission registers 12 are in turn coupled to a parallel to serial converter 14 wherein all signals received on

parallel data lines are converted to serial format under clock control (clock not shown). The output of the parallel to serial converter 14 is applied to a modulator and precompensator circuit 16. The modulator and precompensator 16 is operative to convert serial digital signals to digital pulses, each pulse according to the invention being generated with sufficient energy to optimize slew rate between consecutive pulses as explained hereinafter. The implementation of the modulator portion of the circuit 16 would be apparent to the ordinarily skilled technician given the specification of output characteristics. The modulator/precompensator circuit 16 may optionally be under the control of a sequence controller 18. The sequence controller 18 monitors the input pattern and instructs the modulator precompensator 16 as to the amount of energy, represented by amplitude, to be included in each pulse.

The output of the modulator/precompensator circuit 16 is applied to an output coupling through a pulse transformer 20 across a balanced load, including resistors R1 and R2. The pulse transformer 20 comprises a center tapped primary winding 21 with terminals 131, 133 and 134 and a pair of biased secondary windings 23 and 25, the first secondary winding being coupled to a first lead 24 of a twisted-pair cable 22 and to a negative DC bias supply (for example, -48 volts DC), and the second secondary winding being coupled to a second lead 26 of the twisted-pair cable 22 and being coupled to zero volts DC. The DC connection is for supplying power to a remote station through direct coupling. Signal coupling between the two secondary windings 23 and 25 of the pulse transformer 20 is by means of a coupling capacitor 28. Thus the AC signal is completely decoupled from a DC power supply.

Received signals applied to the twisted-pair cable 22 are routed to taps 30 and 32 on the primary winding 21 of the pulse transformer 20.

The twisted-pair cable 22 is connected to a remote transceiver (not shown). Since the receiver section of the

transceiver 10 is identical, attention is directed to receiver section 33 of transceiver 10. Differential receiver elements 34 receives threshold set signals through a threshold controller 36. The threshold controller 36 may be a fixed voltage source or it may both detect voltage level on the taps 30 and 32 and generate a voltage reference level on reference line 38. The nominal voltage reference level is preferably amplitude sensitive and referenced to the average power or amplitude between positive-going and negative-going pulses. Such threshold setting is conventional and therefore not described herein detail as it is not pertinent to the claimed invention. Reference line 38 is coupled to reference inputs 40 and 42 of the receivers 34. The receiver element 34 generates two signals RI+ at output 44 and RI- at output 46. Outputs 44 and 46 are connected to a data recovery and synchronization logic circuit 48. The logic circuit 48 may employ an internal clock or as additional input a high frequency clock of a rate of at least six times faster than a minimal bit rate in order to drive internal timers as hereinafter explained. Logic circuit 48 is also coupled to the sequence controller 18. The implementation of the logic circuit 48 will be explained hereinafter.

Output of the data recovery and synchronization logic circuit 48 is a serial pattern representing the data recovered from alternate marked inverted (AMI) encoded data. This output is applied to a serial parallel converter 50 which in turn is applied to receive registers 52. The receive registers 52 provide, for example, eight data output lines, a frame sync line and a timing clock line which may be used for further processing in accordance with the defined packet format. The details of the packet format need not be discussed herein since the invention is directed merely to operation within limits imposed by a packet environment, namely, a ping-pong protocol requiring rapid and frequent synchronization acquisition.

It is helpful to understand the coding technique and the code recovery technique. For this purpose, reference is made to Figures 4A through 4C. Figures 4A through 4C are waveform diagrams on a common time scale representing, respectively, a transmitted waveform 200, a received waveform 300 and a data window waveform 400 employed to detect the received waveform. Underlying the data window waveform 200 is a high-speed, high precision clock signal which for example is operative at six times the rate of the signal represented by the data window waveform 400. A data window such as window A, is enabled for a period of one-half cycle. Hence, such a high-speed clock produces three complete cycles for six transitions during each data window. The number of transitions per data window represents the phase resolution as hereinafter explained.

Figure 4A illustrates transmitted AMI encoding wherein pulses correspond to logic ONES and the absence of pulses corresponds to logic ZEROES. The pulses according to the present invention are of invariably alternate polarity. In accordance with the invention, AMI encoding herein must involve the total absence of intentional bipolar violations.

Referring to Figure 4B, there is shown a representation of a received waveform 300, that is, a signal applied to the transmission medium which has become subject to intersymbol interference because of bandwidth limitations of the medium. If the time interval between adjacent pulses is less than the complete discharge time of a pulse applied to the transmission medium, intersymbol interference will occur. The effect shown in Figure 4B is that of a received waveform on an exemplary twisted-pair cable at a data rate of greater than 0.5 M bit/sec. over a distance of greater than about 200 meters from a transmitter transceiver. As will be evident, the received waveform does not settle to a zero value for periods greater than the allowable time between symbols, as represented by HIGH, or ENABLED, states A, B, C, D, etc., of the data window waveform 400 (Figure 4C).

According to the invention, therefore, a dual threshold scheme is employed wherein the threshold for distinguishing between a pulse and the absence of a pulse is modified in accordance with signal reception history and a knowledge that the transmitted waveform contains no bipolar violations. For example, at the outset of reception, either a threshold 310 or a threshold 320, when exceeded by energy in a received signal, would indicate reception of a pulse. In the example shown, threshold 310 is first encountered during data window state A. Circuitry as hereinafter explained, disables threshold 310 and retains threshold 320 by the time of the next data window state, data window state B. During data window state B, a pulse is detected indicating a logic ONE value. Threshold 320 is a mirror or complementary value of threshold 310 with respect to a dc reference level 330.

The threshold following data window state B inverts since a pulse has been detected. Hence, threshold 310 is reinstated during data window state C, indicating that a valid pulse must contain enough energy to overcome the effects of intersymbol interference with prior symbols. Had the threshold not been inverted during data window state C, a zero reading would have been falsely read as a pulse because of intersymbol interference. With the next occurrence of a pulse exceeding threshold 310 (during data window state D), the threshold 310 is again inverted to restore threshold 320. Threshold 310 remains masked until a negative going pulse exceeds threshold 320, which occurs during data window state I. The threshold 310 again inverts so that during data window state J, a pulse is detected. Thereafter, the threshold again inverted so that during data window state K, a false reading is avoided.

Referring to the waveform diagrams of Figures 4B and 4C, data window state A is synchronized to the first occurrence of the received waveform exceeding either threshold 310 or threshold 320. Hence data window state A is enabled for a predetermined period only after the

occurrence of a pulse exceeding either one of the thresholds 310 or 320. The relative timing of the data window state A as well as all subsequent data window states is determined by an underlying high-speed clock. A signal exceeding either threshold 310 or threshold 320 causes data window state A to be enabled at the next transition of the underlying high-speed clock. Thus the resolution of a data window with respect to the received waveform is relative to the nearest subsequent transition of the high-speed clock. Since there are two possible transitions relative to the beginning of a data window, synchronization may either be to the threshold immediately preceding or immediately after the occurrence of a received data pulse.

The high-speed clock is preferably derived from a high precision oscillator. Synchronization of a stream of bits is frame-oriented. In the particular embodiment herein disclosed, synchronization acquisition occurs each 125 microseconds. Synchronization acquisition according to the invention is to occur at the first pulse after the beginning of each frame. If there is period of time of at least five microseconds, pulses will not be effected by intersymbol interference and therefore the leading edge of the first pulse in a series is used to enable the first data window. Synchronization is thereafter a matter of concern only if the local clock is operative at a clock rate which is out of intended tolerance. Moreover, it is contemplated that only a fraction of the 125 second frame will be used for the transmission of information. Hence, high precision oscillators provided at each node in the system and which operate at the same nominal frequency may be used for local control of data windows. A universal clock is unnecessary so long as local clocks are synchronized to the beginning of each frame. As an example of the amount of drift which might be expected in an actual system, consider two oscillators wherein one oscillator is provided at a central switching node and the other oscillator is in a remote device at a termination node. If each of the oscillators

have a precision of 50 ppm, then the maximum drift in a frame period of 125 microseconds is a mere 12.5 nanoseconds. This amount of drift is well within permissible limits for frame synchronization. In reality, accuracy is much greater because only a fraction of the 125 microseconds frame is generally used, and synchronization acquisition following a period of idle time does not occur until the actual transmission of data.

According to the invention, synchronization acquisition is achieved by the use of a shift register in connection with a high precision counter. The conventional synchronization acquisition technique has been the use of a precision phase-locked loop. The acquisition time of a phase-locked loop is substantially longer than the acquisition time of the present invention, and the precision achievable with a conventional phase-locked loop system is no greater than the precision achievable with the present invention.

Reference is made to Figure 2 which illustrates the logic circuits used to overcome intersymbol interference and to acquire synchronization. The outputs 44 and 46 of comparators 34 (Figure 1) are inputs to the data recovery and synchronization logic 48 (Figure 2). A high-speed clock 54 is coupled to clock inputs of first shift register 56 and second shift register 58. The high-speed clock 54 is operative at a rate preferably at least six times faster than the minimal bit rate of the data to be recovered. The high-speed clock 54 is driven by a high precision oscillator 60, as hereinabove explained. The high-speed clock 54 and the high precision oscillator 60 need not be unique to the data recovery and synchronization logic circuit 48 but may be shared with other elements of the transceiver requiring a digital clock. The logic circuit 48 further includes a bistable multivibrator or flip-flop 62, a first AND gate 64 and a second AND gate 66, each of the respective AND gates 64 and 66 having an output coupled to data inputs of shift registers 56 and 58. Each of the shift registers 56 and 58

has two outputs, a first feedback output through respective inverters 68 and 70 and a synchronization output 72 and 74 to an OR gate 76. The output of the OR gate 76 is a synchronization bit signal applied to the clock input of a flip-flop 78.

While the threshold masking operation of the logic circuit 48 of Figure 2 would be apparent to one of ordinary skill, an explanation of operation is instructive. Before the start of the receiving phase of the logic circuit 48, a frame signal FRM on signal line 90 coupled to one of the three inputs to both NAND gates 80 and 82 forming the flip-flop 62 is preset to a logic ZERO by a set signal to the set input s of flip-flop 78. Consequently, both outputs of flip-flop 62 are set to logic ONE. The AND gates 64 and 66 will then produce an output when either input 44 or input 46 becomes active. The state of the output of AND gates 64 and 66 is shifted continuously through the shift registers 56 and 58 under control of the high-speed clock 54. At the occurrence of a signal exceeding the threshold set by threshold controller 36, either input 44 bearing signal RI+ or input 46 bearing signal RI- produces a logic ONE at the data input of one or the other of serial to parallel shift registers 56 or 58. Data will be shifted through the activated shift register until picked off by either feedback output through inverter 68 or feedback output through inverter 70, represented respectively as R2 compliment or R1 compliment. The R2 compliment signal is fed back to the R2 compliment input of NAND gate 82. The R1 compliment signal is fed back to R1 compliment input of NAND gate 80. The generation of these compliment output signals is at a fixed finite delay following the introduction of a signal at the data input, depending on the position within the shifted register from which the data is derived.

When a signal from the signal lines 44 or 46 is applied to either of the AND gates 64 or 66, the respective signal is propagated to the input of the shift register 56 or 58, since the outputs of both NAND gates 80 and 82 are

initially high. The signal is propagated through the shift register to the output tap. For example, if a signal RI+ is enabled to apply a logic ONE to the data input of the shift register 56, a signal R2 compliment is generated through inverter 68 to be applied to one of the inputs of NAND gate 82. Initially, such a signal has no effect because the frame signal line 90 is at a logic ZERO level. However, the data signal in shift register 56 is further propagated to output line 12 through the OR gate 76 to the clock input of the flip-flip 78. The data input of the flip-flop 78 is preset at terminal Z to a logic ONE (+5 volts). Thus, when a logic ONE is applied at the clock input of the flip-flop 78, the output on frame line 90 changes to a logic ONE, which in turn is applied to the inputs of the NAND gates 80 and 82. As soon as the frame signal FRM on line 90 goes to a logic ONE, the output of the NAND gate 80 goes to a logic ZERO thereby causing the output of AND gate 64 to go to a logic ZERO. Therefore, according to the invention, any signal on input 44 is thereby masked from the shift register 56. Shift register 58 remains responsive to input signals applied through input 46, since the output of NAND gate 82 remains at logic level ONE so long as one input remains at logic level ZERO. In this case, the output of NAND gate 80 is cross-coupled to one of the three inputs of NAND gate 82, thereby forcing the output of NAND gate 82 to remain at a logic ONE level. After a predetermined number of cycles, the R2 compliment signal reverts to a logic ONE state as the logic ZERO of the data input of shift register 56 propagates through the shift register. The logic circuit 48 then expects to receive the next pulse indicating a digital ONE at input 46. If no pulse signal is received at input 46 during the period specified for a data window, the circuitry interprets the signal as a digital ZERO. However, if a signal is applied to input 46 which is a digital ONE, such signal is propagated through the AND gate 66 to the shift register 58 which in turn after a predetermined period manifests a logic ZERO on the R1 compliment output to the

NAND gate 80. The NAND gate 80 is then forced to a logic ONE state which in turn forces NAND gate 82 to a logic ZERO state to mask signals applied at input 46 from the shift register 58. In this manner, the duration of each pulse is made independent of the actual duration of the pulse on the transmission medium, and the initial threshold polarity with respect to a neutral reference is determined by the initial data pulse on the transmission medium.

Referring again to Figure 2, there is shown a data window circuit 92 in accordance with the invention. The data window circuit 92 comprises a serial to parallel shift register 94 coupled with a clock adapter circuit 96. The purpose of the clock adapter circuit 96 is to provide a clock signal at both the leading edge and the trailing edge of each output of the high-speed clock 54 in a polarity consistent with the polarity of the initial pulse and all subsequent signal pulses.

The shift register 94 is coupled to receive at its CLEAR input the frame signal FRM on line 90 and the CLOCK signal from the clock adapter circuit 96. In a specific embodiment, the third output tap of the shift register 94 is feedback coupled through an inverter 98 to input terminal 100 of the shirt register 94. The output of the shift register is a data window signal on a line 102 to a dual input NAND gate 104. The NAND gate 104 receives as its other input the sync bit signal from OR gate 76. The output of the NAND gate 104 is the desired data output signal (Figure 5E) occurring during a valid data window state (Figure 5D). Referring particularly to Figure 5A, 5B, 5C, 5D and 5E there is shown an example of the timing sequence associated with the shift register 94. In Figure 5A, the sync bit signal provided as the output of OR gate 76 is shown. On the trailing edge of the sync bit signal, the frame signal is generated on line 90 (Figure 5B). The frame signal is fed to the clear input of the shift register 94 (Figure 2) to clear the shift register 94 of all residual data. A clock signal on a line 106 out of the clock adapter

96 produces a signal employed to drive the shift register 94. In a preferred embodiment, the shift register 94 responds to a positive leading edge clock. After a predetermined number of clock cycles, (in the particular embodiment shown here, after three cycles,) an output signal on a line 102 is provided from the shift register 94. This is the data window signal provided both to the NAND gate 104 and to the inverter 98. The output of the inverter 98 is fed back to the input 100 of the shift register 94. Referring to Figure 5D, the data window signal is enabled in response to a positive going edge of the clock (Figure 5C) and is disabled in response to a subsequent positive going edge. The ANDing of the data signal on the sync bit line (Figure 5A) with the data window signal (Figure 5B) produces an indication of the presence of a pulse (indicating a digital ONE) or produces an indication of the absence of a pulse (indicating a digital ZERO) in the received signal.

Referring with greater detail to the clock adaptor 96, there is shown a first flip-flop 108 and a second flip-flop 110 having outputs coupled through AND gates 112 and 114 respectively, the outputs of which are coupled to an OR gate 116 which produces an output signal to clock line 106. The flip-flops 108 and 110 are each driven by the high-speed clock 54 in inverted relationship to one another as determined by an inverter 118. The clock 54 as inverted also drives the second input of AND gate 114. The noninverted clock signal drives the second input of AND gate 112. The data input of each of the flip-flops 108 and 110 is the sync bit signal from the OR gate 76. The complementary outputs of the flip-flops 108 and 110 are cross-coupled respectively to the CLEAR inputs of the other flip-flops 110 and 108. The circuit elements thus cooperate to provide a leading edge clock input signal in phase and synchronous with the first bit of data in each frame.

Figure 3 shows a diagram of a precompensation circuit 120 for providing transmission precompensation in accordance with the invention as may be employed in the

modulator precompensator 16 of Figure 1. Only the precompensation circuitry 120 is of interest here as the other circuits used therein are conventional and need not be described to the ordinarily skilled technician.

Precompensation circuitry 120 constructed in accordance with the invention is for the purpose of transmitted pulses in such a way that the effect of intersymbol interference produces a minimal effect on data recovery at the receiving end of a transmission medium such as a twisted-pair cable. Precompensation is implemented in a bit-by-bit fashion to maximize intersymbol slew rate by taking into consideration the previous two transmitted bits and applying a precompensation signal to the next subsequent bit based on a knowledge of the pattern of the previous two bits.

Referring in particular to the elements of Figure 3, data is received from a previous stage in a serial to parallel shift register 122, the output of which is coupled in parallel to the most significant (MSB) address inputs of a programable read only memory PROM 124. Least significant bit (LSB) addresses are provided through a counter driven by a local high frequency clock 154. The local high frequency clock 154 is preferably the same clock as used elsewhere in the receiver. The output of the PROM 124 is preferably at least three data bit lines coupled to a shift register 126. The data output thus provides options for eight definable dynamic levels and durations for use in subsequent processing. Specifically, the register 126 is a shift register operative as a latch wherein data from PROM 124 is loaded, the output terminals of which are each coupled to drive loading resistors 128 supplying pulses to the pulse transformer 20 (Figure 1). (The pulse transformer in Figure 3 is shown merely for clarity and is not part of the precompensator circuit 16.)

In a particular embodiment, the register 126 provides four outputs, each output tied through a resistor R3, R4, R5, R6, one terminal of each resistor being coupled to one or the other of the primary input terminals of the

pulse transformer 20. Specifically, a first output resistor R3 is coupled between the first input 21 of the primary winding of the pulse transformer 20 and a first output 130 of the register 126. A second output resistor R4 is coupled between input 21 and a second register output 132. A third resistor R5 is coupled between input terminal or tap 134 of the transformer 20 and a third output 136 of the register 126. A fourth output resistor R6 is coupled between the input tap 134 and a fourth output 138 of the register 126. Resistor R3 is preferably of the same value as resistor R5, and resistor R4 is preferably of the same value as resistor R6 in order to preserve balance across the primary winding of the transformer 20.

The precompensation circuit 120 operates as follows:

At the beginning of a cycle, a two MHz or other data speed clock clears the counter 125 to zero count and begins to clock data to the serial to parallel shift register 122. A high frequency clock 154 clocks the counter 125 at a rate which is a multiple of the two MHz input clock causing the least significant bit (LSB) addresses in the ROM 124 to access stored data regarding pulse and duration amplitude.

With a appropriate subsequent clock pulses of the two MHz clock to the shift register 122, the data applied to the shift register 122 is fed to the most significant bit (MSB) addresses of the ROM 124. Subsequent clocks will shift the data through the shift register 124 thereby changing the MSB bit pattern of the address portion of the ROM 124. Thus the input data is used to select sectors of the ROM 124 for accessing data in accordance with a sequence of counts generated by the counter 125. Data contained in each of the ROM sectors is preselected for timing and amplitude characteristics determinative of desired compensation effects to be applied to the output network of the transmitter. For example, one or more sectors may contain null data, another sector may contain data

representing specific lengths and pulse amplitude combinations (pulse shape). Sectors are addressed based on the current and immediately preceding historic combination of bits applied to the data input of the shift register 122. For example, for input data represented by three consecutive ones, a sector would be addressed which would allow the least significant bits to address data representing a data pattern representing a high amplitude relatively short pulse. Signals would be applied to the resistors R3, R4, R5 and R6 in the combination specifying maximum amplitude. The pulse would be terminated by null data at the last address locations in the addressed sector. Analog signals would be applied for a time dependent on the number of non-null bit contained in the addressed sector.

A precompensation scheme according to the invention is based on a digital pattern intended to increase slew rate by increasing maximum amplitude and minimizing pulse length based on immediately prior history of pulses. A three level logic decision is made.

A pattern according to a specific embodiment of the invention herein is as follows:

If the current transmitted bit is a one (a pulse) and the immediately preceding two bits are zeros (no pulses), the pulse generated by the ROM data is a low amplitude pattern having a long duration. If the current transmitted bit is one, the first immediately preceding bit is one and the second immediately preceding bit is zero, then the pattern presented by the ROM-stored data bits is a medium amplitude pattern having a medium pulse length. If the current transmitted bit is a one and all immediately preceding bits are one, then the pattern presented by the ROM-stored data bits is a high amplitude relatively short pulse. If the current bit is a one, the immediately preceding bit is a zero and the second immediately preceding bit is a one, the data bits represent a medium amplitude pulse of intermediate length. The object is to provide the same total energy in each pulse.

The invention has now been explained with reference to specific embodiments. Other embodiments will be apparent to one of ordinary skill in this art. It is therefore not intended that this invention be limited except as indicated by the appended claims.

CLAIMS

I CLAIM:

1. An apparatus for transmission and reception of digital data over a bandlimited channel comprising:

means for generating and transmitting pure alternate mark invert pulse code signals from digital message signals; and

means for receiving and detecting alternate mark invert pulse code signals, said detecting means being operative to recover said digital message, said detecting means including means defining two detection thresholds and means alternately masking said detection thresholds upon receipt of a signal representing a pulse in order to minimize effects of intersymbol interference.

2. An apparatus for transmitting and receiving digital data over a bandlimited channel comprising:

means for generating and transmitting pure alternate mark inverted code from a digital message signals, said generating and transmitting means including means for digitally precompensating generated alternate mark inverted pulse code signals prior to transmission based on preceding signals for suppressing the effects of intersymbol interference on received pulse signals and for simplifying detection; and

means for receiving and detecting alternate mark invert code pulse signals to recover said digital message.

3. The apparatus according to claim 1 wherein said generating and transmitting means includes means for digitally precompensating amplitude and duration of generated alternate mark inverted pulse code signals based on digital values of preceding message signals in order to minimize effects of intersymbol interference in received signals.

4. The apparatus according to claim 3 wherein said precompensating means comprises means operative to select length and duration of each transmitted pulse signal to maximize slew rate while maintaining approximately equal energy content among pulses.

5. The apparatus according to claim 3 wherein said digital precompensating means comprises:

a shift register for receiving said message signals;

a programable read only memory coupled to receive outputs said shift register as most significant bit addresses for selecting sectors of said memory means;

a digital counter coupled to least significant bit addresses of said memory means for generating a sequence of addresses to read out data in sectors selected by message signals to said shift register; and

means for converting said data from said sectors of said memory means to analog signals of amplitude and duration determined by said data.

6. The apparatus according to claim 1, 2, 3, 4, or 5 wherein said receiving and detecting means includes digital means for acquiring synchronization of data windows to each first one of said received pulse signals, said received pulse signals being in a packet format of limited duration, said synchronization acquiring means including a local high precision clock for maintaining synchronization for said limited duration.

7. The apparatus according to claim 6 further including means for selecting between a first detection threshold value favoring pulse signals of a first polarity and a second detection threshold value favoring pulse signals of a second polarity reverse of said first polarity, said selecting means being based on polarity of said first one of said received pulse signals.

8. The apparatus according to claim 1 further including means for selecting between a first detection threshold value favoring pulse signals of a first polarity and a second detection threshold value favoring pulse signals of a second polarity reverse of said first polarity, said selecting means comprising means for sensing polarity of each first one of said received pulse signals and in response to sensed polarity masking receipt of subsequent pulse signals of the same polarity until a pulse signal of reverse polarity is sensed.

9. The apparatus according to claim 8 further including means for selecting polarity of a local high-speed clock in response to polarity of said first one of said received pulse signals.

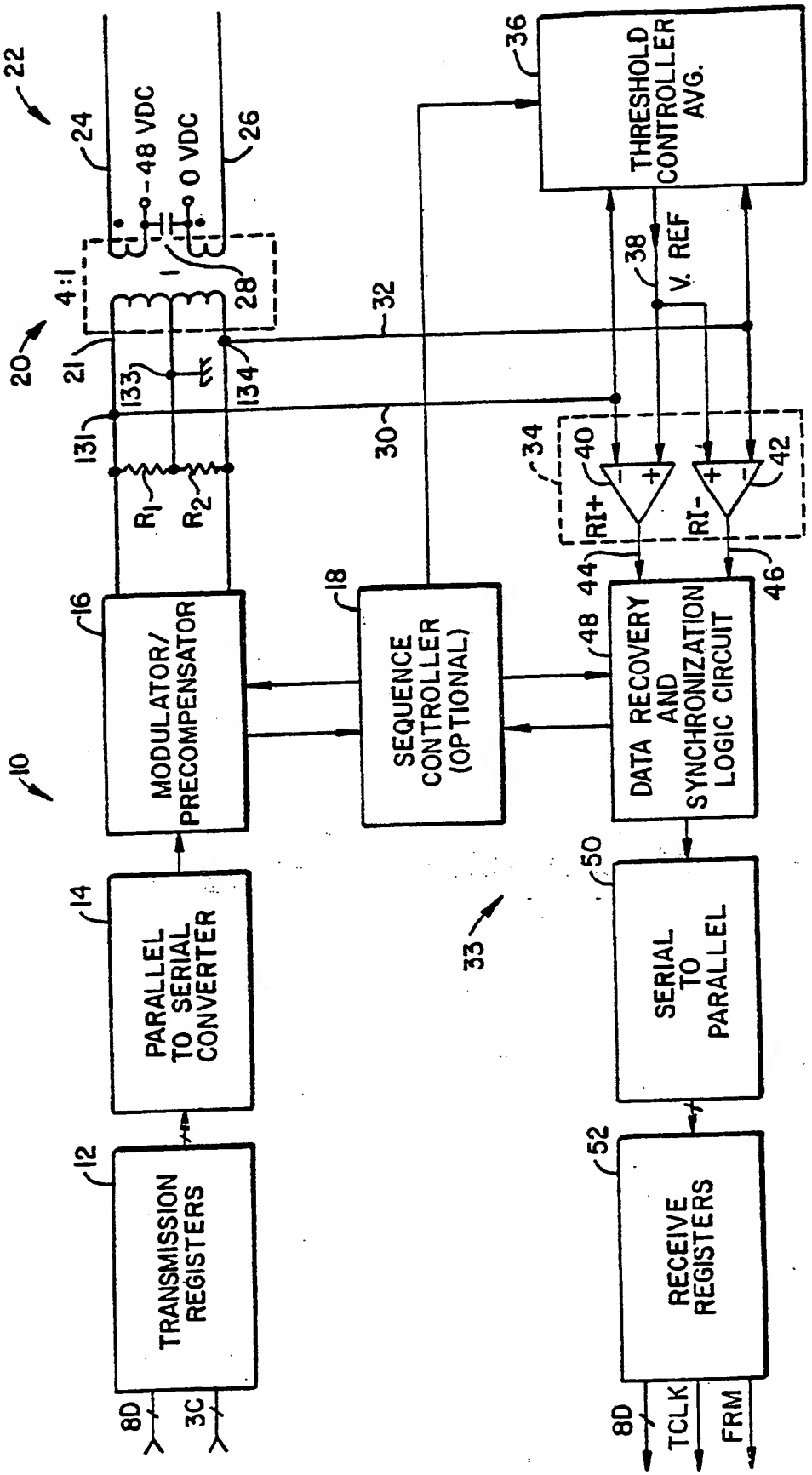

FIG. 1.

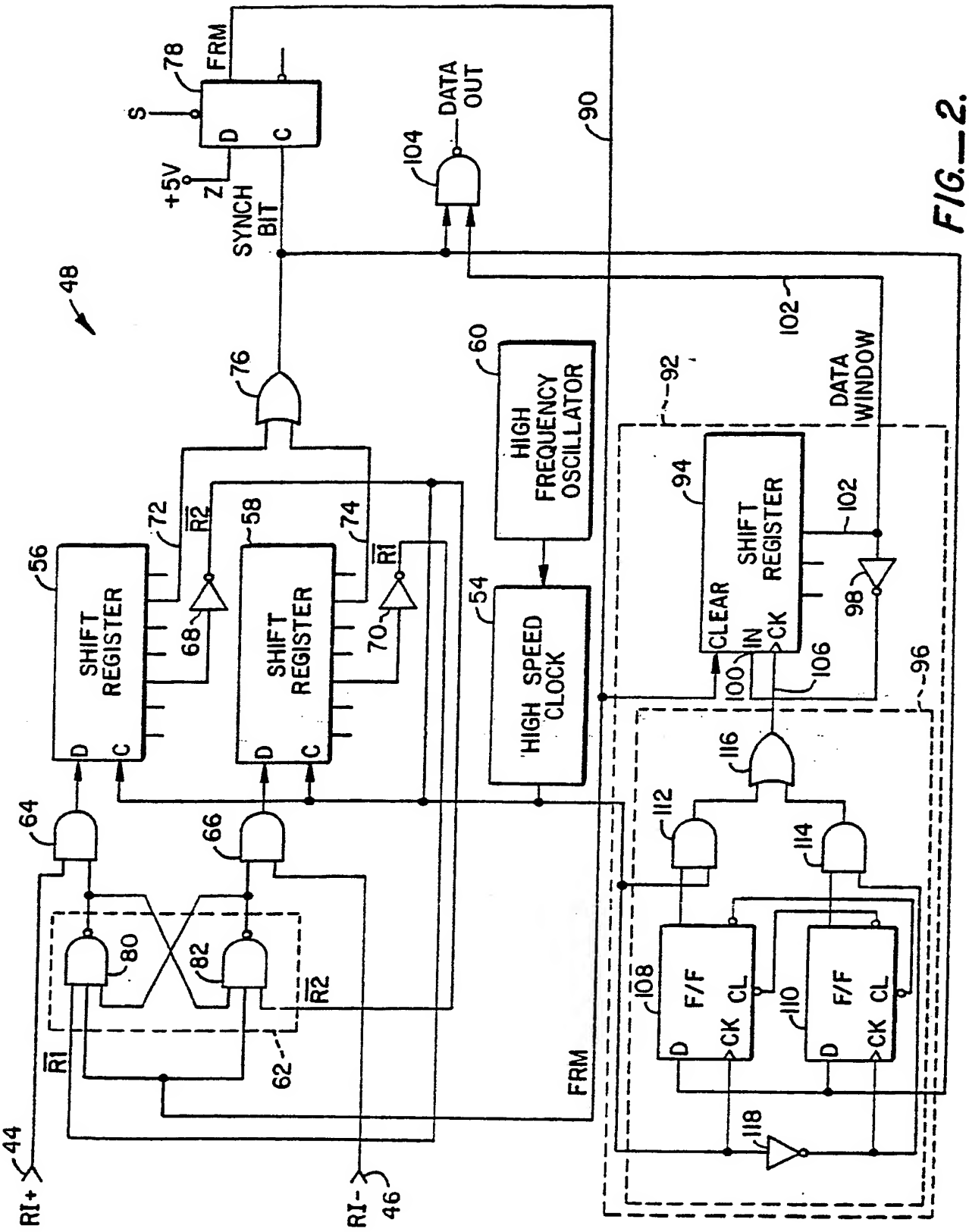

FIG._2.

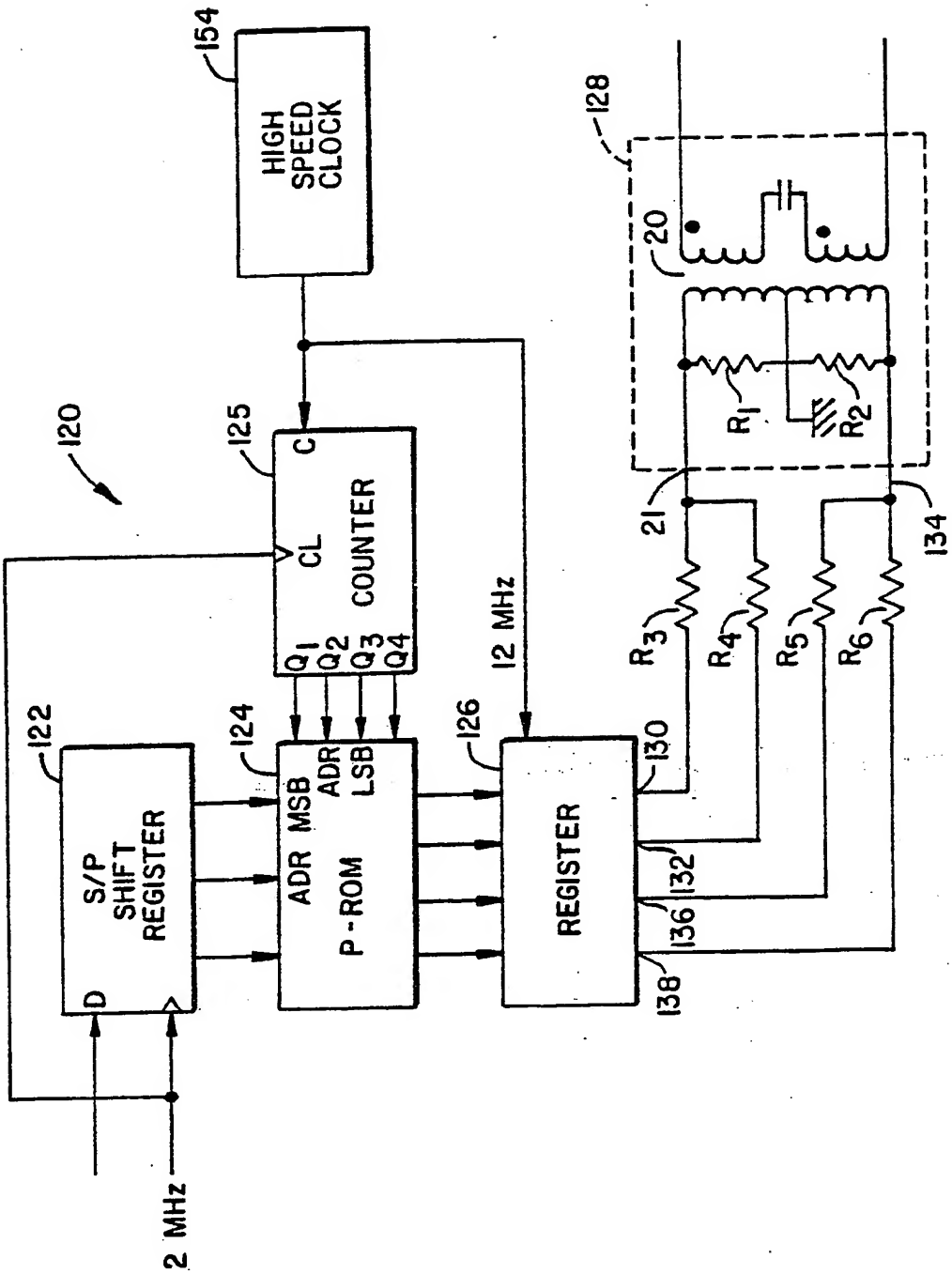
154
HIGH SPEED CLOCK
128
20
120
125
C
CL
COUNTER
Q1 Q2 Q3 Q4
12 MHz
R1
R2
21
134
R3
R4
R5
R6
122
124
126
130
S/P SHIFT REGISTER
D
ADR MSB
ADR LSB
P-ROM
REGISTER
132
136
138
2 MHz

FIG_3.

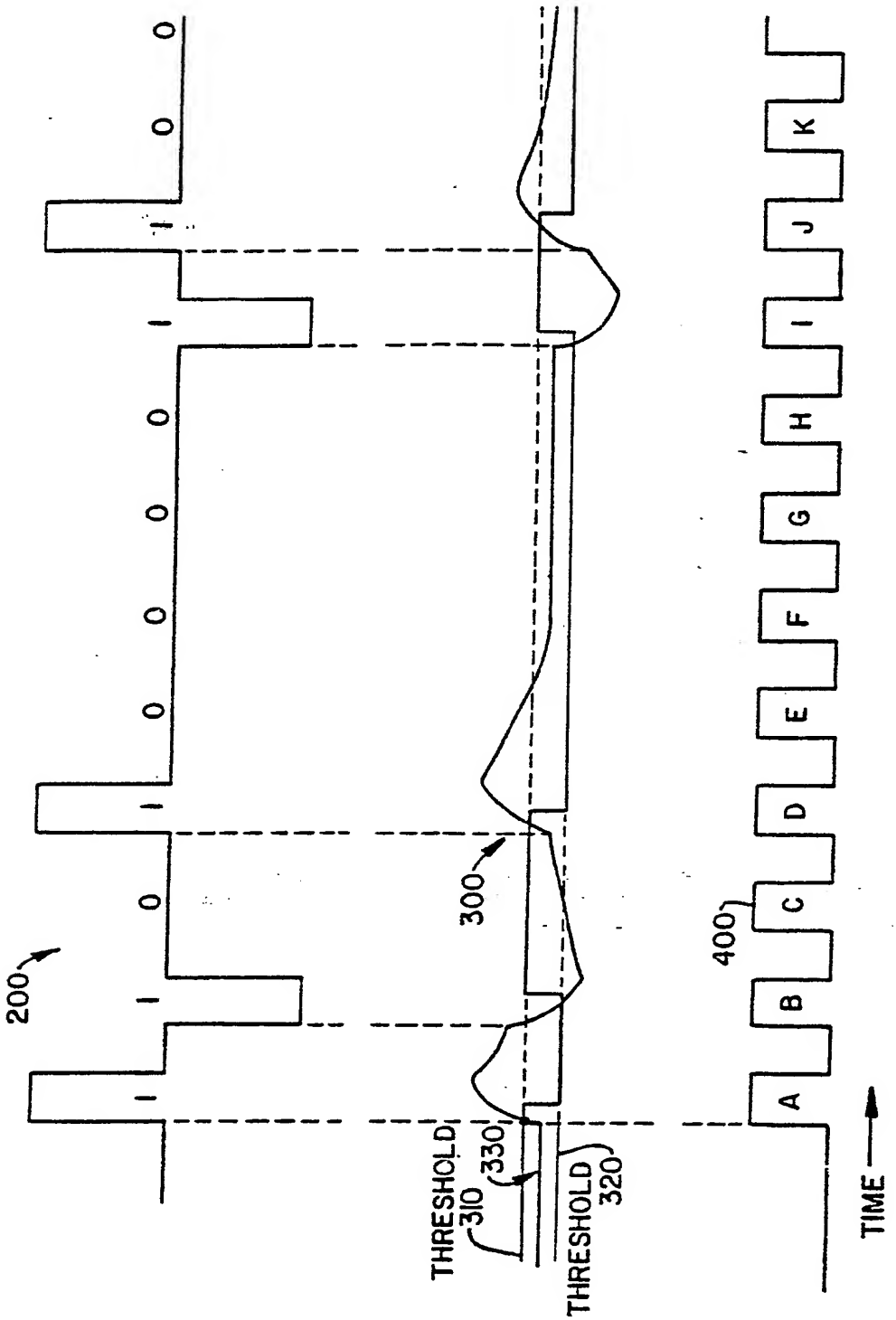

FIG._4A. FIG._4B. FIG._4C.

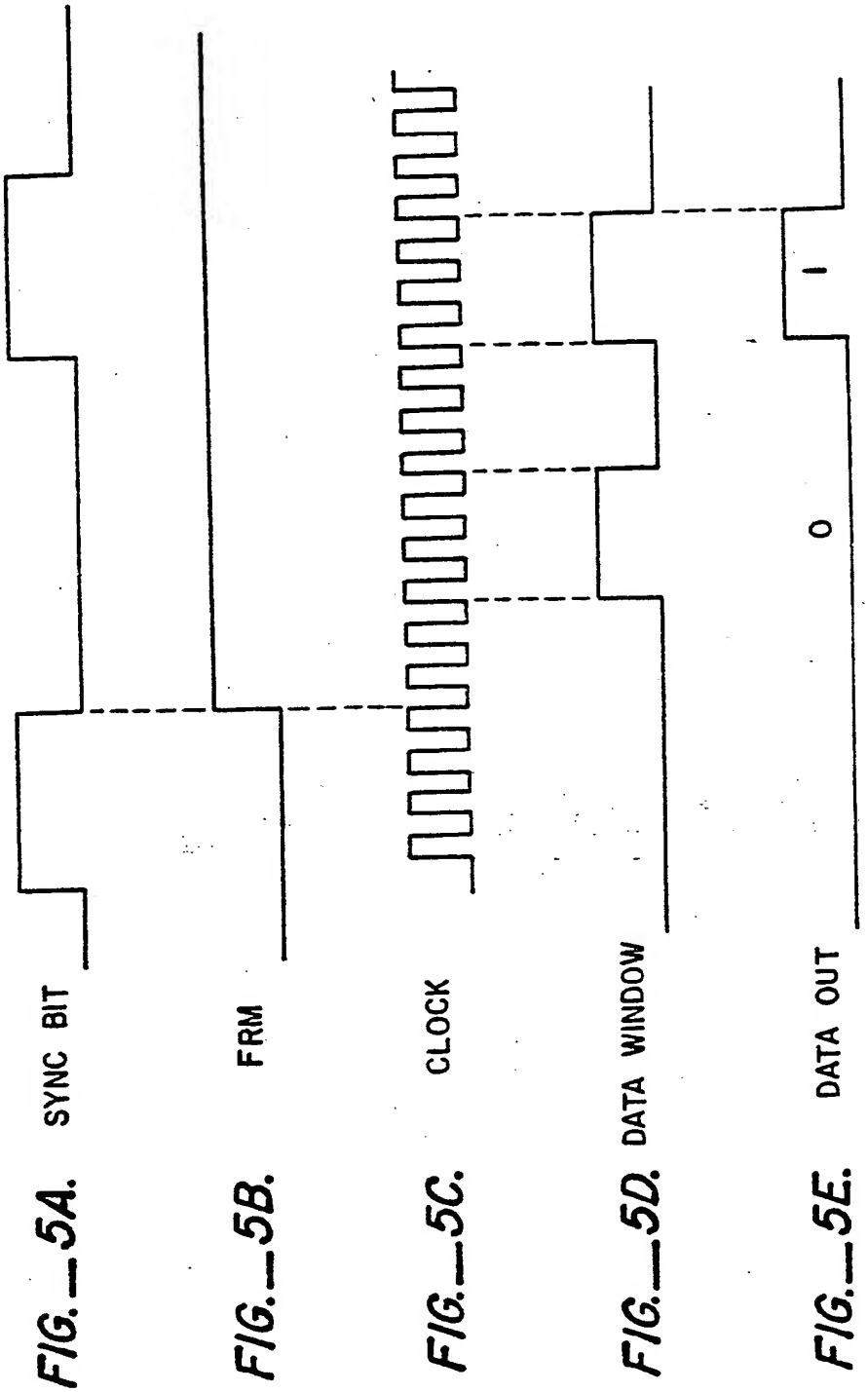

FIG._5A. FIG._5B. FIG._5C. FIG._5D. FIG._5E.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US85/00524

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. CL[3] - H03K 6/04; G01R 19/165; H03L 7/00
U.S. CL - 307/360; 360/40; 375/20,60,76,110

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	375/18, 20, 34, 60, 76, 95, 101, 110; 360/40, 43; 307/360.

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,007,382, 08 February 1977, Warberg	1-9
Y	US, A, 4,071,692, 31 January 1978, Weir et al	1-9
Y	US, A, 4,339,724, 13 July 1982, Feher	2-7
Y	US, A, 4,041,239, 09 August 1977, Haass	4,6,7
Y	US, A, 4,291,277, 22 September 1981, Davis et al.	5
Y	US, A, 3,824,498, 16 July 1974, McBride	5
Y	US, A, 4,157,509, 05 June 1979, Zielinski	1-9
Y	US,A, 3,459,964, 05 August 1969, Yoshida et al.	1-9

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
01 May 1985	11 JUN 1985
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Raymond C. Glenn

ORIGINAL

NO MARGINALIA

Form PCT/ISA/210 (second sheet) (October 1981)